Tribhuvan University

Faculty of Humanities & Social Sciences

OFFICE OF THE DEAN

2025

Bachelor in Computer Applications
Course Title: Digital Logic
Code No: CACS 105
Semester: I

Full Marks: 60
Pass Marks: 24
Time: 3 hours
Batch: 2024

Candidates are required to answer the questions in their own words as far as possible.

Group B

Attempt any SIX questions. **[6×5 = 30]**

2. Define analog and digital quantities. Subtract: 1010101.101 – 1000100.001 using both 1's and 2's complement. [1 + 2 + 2]
3. Convert $(2594.68)_{10}$ into hexadecimal number. Design full subtractor with its block diagram, truth table, logic diagram and Boolean expression. [2+3]
4. What NAND and NOR gates are called universal gates? Express the Boolean function F(A,B,C,D) = D(A'+B) + B'D into standard SOP and POS. [1+2+2]
5. Combinational circuit that generates 9's complement of a 3 input numbers and implementing it using 3 gates only. Design 1:8 DEMUX using 1:4 DEMUX and 1:2 DEMUX. [3+2]
6. Define state table. Design a combinational circuit using a ROM. The circuit accepts a 3-bit number and generates an output binary number equal to the square of the input number. [1+4]
7. Design Mod-11 synchronous counter. [5]
8. How flip flop differs from latch. Explain clocked SR flip flop with logic diagram, truth table, characteristic table and excitation table. [1+4]

Group C

Attempt any TWO questions. **[2×10 = 20]**

9. Differentiate between PAL and PLA. Design a combinational circuit with four inputs that represent a decimal digit in BCD and four output lines that generate the 2's complement of the input binary patterns with circuit diagram, truth table and block diagram. [4 + 6]
10. Define multiplexer. Explain 4:1 multiplexer with its block diagram, truth table and logic diagram. Implement 8:1 multiplexer with using lower order multiplexer. [2+4+4]
11. Explain how race condition in JK flipflop can be resolved? Design a 3-bit gray code synchronous counter. [4+6]