Tribhuvan University

Faculty of Humanities & Social Sciences

OFFICE OF THE DEAN

2024

Bachelor in Computer Applications
Course Title: Digital Logic
Code No: CACS 105
Semester: I

Full Marks: 60
Pass Marks: 24
Time: 3 hours

Candidates are required to answer the questions in their own words as far as possible.

Group B

Attempt any SIX questions. **[6×5 = 30]**

2. Define Digital computer. Subtract: 1010101.101 – 1000100.001 using both 1's and 2's complement. [1 + 2 + 2]
3. What do you mean by K-map? Explain the K-map with three variables. Simplify F(p,q,r,s) = ∑(3,4,7,8,14) which has the don't care conditions d(p,q,r,s) = ∑(1,6,9,13) and design the logic circuit using minimum number of NAND gates. [1+2+2]
4. Differentiate between combinational logic circuit and sequential logic circuit. Implement a full adder circuit using decoder and two OR gates. [2 + 3]
5. Define priority encoder. Explain 8 to 3 priority encoder in detail. [1 + 4]
6. Explain the duality theorem with example. Draw a logic gates that implement following expression. [2+1.5+1.5]

   F = AB + CB D' + B' C

   F = (A + B) (B' + C) + A (C' + D + E)
7. How flip flop differs from latch. Explain clocked SR flip flop with logic diagram, truth table, characteristic table and excitation table. [1+4]
8. Write short notes on: (any two) [2.5+2.5]

   a) State reduction table b) Multiplexer c) Synchronous and Asynchronous counter

Group C

Attempt any TWO questions. **[2×10 = 20]**

9. Differentiate between PAL and PLA. Design a combinational circuit with four inputs that represent a decimal digit in BCD and four output lines that generate the 2's complement of the input binary patterns with circuit diagram, truth table and block diagram. [4 + 6]
10. Explain shift register with parallel load. Design a synchronous Mod-10 counter to count in the sequence 0,2,4,5,6,8 using T flip-flop. [5+5]
11. Explain how race condition in JK flipflop can be resolved? A sequential circuit with two D Flip-Flops, A and B; two inputs, x and y; and one output, z, is specified by the following next-state and output equations: [4+6]

    $A(t+1) = xy' + xB$

    $B(t+1) = x'B + xA$

    $z = A$