Tribhuvan University

Institute of Science and Technology

2066

Bachelor Level/ First Year/ Second Semester/ Science — Full Marks: 60

Computer Science and Information Technology (CSc. 151) — Pass Marks: 24

(Digital Logic) — Time: 3 hours.

Candidates are required to give their answers in their own words as for as practicable.
The figures in the margin indicate full marks.

Long Answer Questions:
Attempt any TWO questions. (2x10=20)

1. Design the 4 bit Synchronous up/down counter with timing diagram, logic diagram and truth table.
2. Design a Full subtractor with truth table and logic gates.
3. Design a decimal adder with logic diagram and truth table.

Short Answer Questions:
Attempt any EIGHT questions. (8x5=40)

4. Differentiate between Analog and Digital system.
5. Convert the following octal numbers to hexadecimal.
   a) 1760.46
   b) 6055.263
6. Which gates can be used as inverters in addition to the NOT gate and how?
7. Draw a logic gates that implements the following
   a) A= (Y1 XOR Y2) (Y3 XNOR Y4) OR (Y5 XOR Y6 XOR Y7)
   b) A = (X1 XNOR X2) OR (X3 XNOR X4) OR (X4 XNOR X5) XOR (X6 XNOR X7)
8. State and prove De-Morgan's theorem 1st and 2nd with logic gates and truth table.
9. Reduce the following expressions using K map
   A' + B(A + B' + D) (B' + C) (B + C + D)
10. Differentiate between a MUX and DEMUX.
11. Explain the operation of Decoder.
12. What are the various types of shift registers?
13. What do you mean by synchronous counter?