## **Tribhuvan University Faculty of Humanities and Social Sciences** Office of the Dean 2019

**Bachelor in Computer Application Course Title: Digital Logic** Code no: CACS 105

figures in the margin indicate full marks.

Semester: I

Candidates are required to give their answers in their own words as for as practicable. The

## Group B

## Attempt any SIX questions.

[6x5 = 30]

Full Marks: 60

Time: 3 hours

Pass Marks: 24

2. Subtract: 1010.110 — 101.101 using both 2's and I's complement.

[5]

3. Simplify (Using k-map) the given Boolean function in both SOP and POS using the don't care condition d:

F (A, B, C, D) = 
$$\Omega(0,1,3,7,8,12)$$
 and  $\Omega d(5,10,13,14)$ 

[2+3]

4. Define decoder. Draw logic diagram and truth table of 3 to 8-line decoder.

[1 + 4][2 + 3]

5. Define ROM. Implement the following combinational logic function using ROM:

A1 A0	F1 F2
0 0	1 0
0 1	0
1 0	1
1	1 0

- 6. What are the drawbacks of clocked RS flip flop? Explain the operation of JK Flip flop along with its circuit diagram and characteristic table. [2+3]
- 7. What is T-Flip-Flop? Explain clocked JK flip-flop with logic diagram and truth table. [1 + 4]
- 8. Design MOD 7 counter with state and timing diagram.

[2 + 1 + 2]

## **Group C**

- 9. Design a PIA circuit with given functions. F1(A, B, C) =  $\Sigma$  (3, 5. 6, 7) F2 (A, B, C) =  $\Sigma$  (0, 2. 4, 7). Design PLA programs table also. [3+7]
- 10. Distinguish between sequential and combinational logic with example. Discuss the design procedure of combinational logic. [4+6]
- 11. A sequential circuit with two D flip-flops, A and B, two inputs x and y, and one output z, is specified by the following next state and output equations
  [4+3+3]

$$\begin{array}{rcl} A(t+1) & = & x'y + xA \\ B(t+1) & = & x'B+xA \\ z=B \end{array}$$

- a. Draw the logic diagram.
- b. Derive the state table.
- c. Derive the state diagram.